The Influence of Heat Treatment on The Magnitude of Mechanical Stresses in The Process of Forming a Field Emission Cathode-Grid Node

Evgeney E. Gusev, Tatiana A. Gryazneva, Alexey V. Negencev and Maksim A. Makhiboroda
National Research University of Electronic Technology
Zelenograd, Moscow, Russia
bubbledouble@mail.ru

***Abstract*— TCAD simulation of the technological process of creating of the cathode-grid assembly, which consists of the field-emission cathode and control-grid electrodes, was performed. The process of forming and sharpening the cathode tip based on a standard batch processing silicon technology is presented. The proposed process flow allows opening self-aligned emitter areas in the grid layer without carrying out high-priced operations of photolithography or mechanochemical polishing. The effect of heat-treatment on the planarity of the Si/SiO_2 surface structure is analysed with the approved method of mechanical stress measurement in PECVD SiO_2 film on a silicon wafer. Based on these results the optimal heat treatment regime is found.**

Keywords*— *X-ray sources, field-emission cathode, mechanical stress, TCAD simulation

I. INTRODUCTION

At present, one of actual problems in modern micro- and nanoelectronics is development of the miniaturized X-ray sources having low power consumption as well as possibility of the tuning of X-ray frequency. This is due to further progress of X-ray techniques for wide range of their practical applications in different fields of science and technology (medicine, analytical equipment and security systems miniature X-ray sources, flat panel displays [1]) which leads to the need for steady improvement of it is key element –X-ray tube. The use of field-emission cathodes can be the effective solution of this issue.

We propose the technological process of formation of cathode-grid system (CGS) consisting of the field-emission cathode and grid control electrodes, enabling to realize the fabrication of the array of field-emission cathodes using batch processing silicon technology. The main feature of the presented route of CGS development is based on the possibility of carrying out opening of the self-combined emitter areas in the grid layer without carrying out expensive operations of a photolithography or chemical and mechanical polishing. One of key parameters which significantly affect the quality of operations of opening of emitter areas is mechanical stress. Mechanical stress can lead to goffering, cracking fissuring and a spalling of deposited films that can lead to the deformation of CGS structure. Besides that, with increasing the bending deflection of the sample the uniformity of the film deposition is decreases. In this connection it is necessary to ensure the continuous improvement of the methods of monitoring and prediction of mechanical stresses appeared in the structure. Thus, work is devoted to the investigation of the influence of heat treatment on the relief of substrate surface on which the CGS structure was formed and to the determination of its mechanical stresses. The considered structure of CGS is formed by the tools of software package Sentaurus TCAD [2], whose technological model can be separated into two technological routes, one for cathode needle and other for CGS formation correspondingly.

II. TCAD SIMULATION OF A TECHNOLOGICAL ROUTE OF FORMATION OF THE CATHODE NEEDLE

The technological route of creation of needle of field emitter allowing group production of array of field-emission cathodes is given below. During the process simulation silicon substrate with crystallographic orientation (100) was used with the atom concentration of phosphorus equal to $1 \cdot 10^{15}$ at./cm^3. At the first step the protective mask was formed on the substrate by thermal oxidation of Si to 0.2 um and further anisotropic deposition of Si_3N_4. Next, operation of photolithography was conducted by anisotropic etching of dielectric layers stopping at Si surface. Anisotropic etching of Si substrate on depth of 1.5 um allows creating pillar which is preform for cathode needle that is shown in Fig. 1.

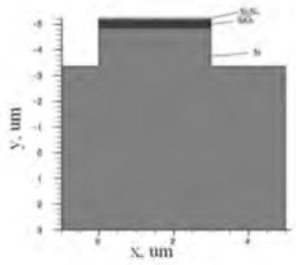

Fig. 1 The formation of Si/SiO_2/Si_3N_4 pillar form after anisotropic etching of layers

The creation of vertical walls of the pillar is carried out similar to the Bosch technology and diameter of the created structure is about 3 um. At the following stage of the route the sharpening of a needle is formed by means of isotropic etching of Si at the depth of 1.2 um after which the long-term dry oxidation is carried out. As a result, a part of the Si material

978-1-5090-4865-6/17/$31.00 ©2017 IEEE

passes into the oxide layer with the thickness of 0.38 um adjacent to the needle surface (Fig. 2).

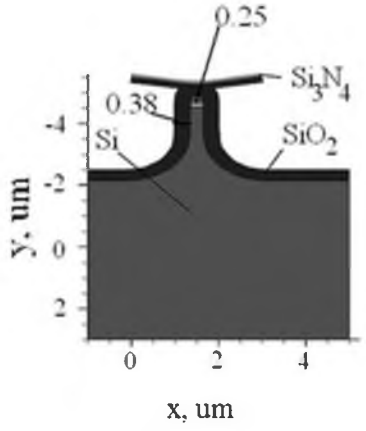

Fig. 2 A form of cathode needle with the surface oxide layer of SiO_2 after operation of dry oxidation

Originally needle thickness is about 0.25 um whereas subsequent removal of dielectric films and isotropic etching of Si at the depth of 0.1 um allows receiving the needle with a small tip shown that is demonstrated in Fig. 3.

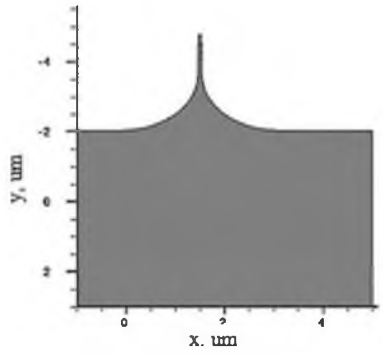

Fig. 3 Structure of the cathode needle at the final stage of a technological route

At the same time, the preliminary diffusion of phosphorus allows reducing the oxidation time and leads to increasing the number of majority charge carriers.

III. Technological Route of Formation of Cathode-Grid System

Further we consider the simulation results of the technological process of CSG formation where the desired profile of the CSG structure can be obtained by means of needle sharpening using the wet thermal oxidation at a temperature 950°C within 50 minutes (Fig. 4).

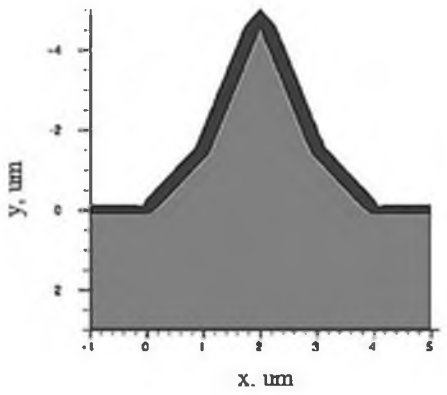

Fig. 4 A form of cathode needle after carrying out the wet thermal oxidation

From Fig. 4 it is visible that the flat area of structure is oxidized more slowly than needle tip. The thickness of silicon dioxide in flat area is about 200 nm. Creation of isolated region between grid control electrodes of Al and cathode requires plasma enhanced chemical vapour deposition (PECVD) of SiO_2 layer with thickness of 1.0 um after which the sputtering of 0.5 um Al film is also carried out. To align the upper boundary of grid control electrodes and the cathode tip and to protect the cathode during the operation, the photoresist layer with 2.25 um thickness is deposited on the structure (Fig. 5).

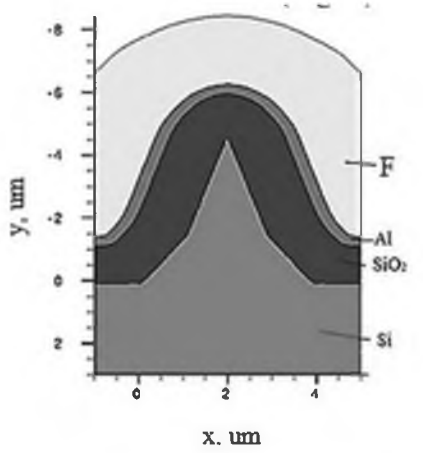

Fig. 5 Structure $Si/SiO_2/Al$/photoresist layer after the deposition

The isotropic etching is made for photoresist layer at the depth of 2.25 um and for Al layer at the depth of 0.5 um correspondingly (Fig. 6a) after which 0.6 um of SiO2 layer is etched (Fig. 6b).

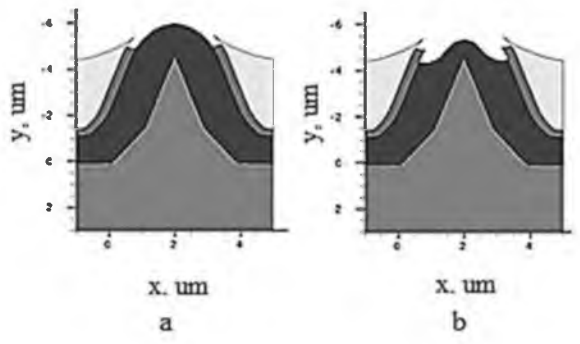

Fig. 6 Structure Si/SiO_2/Al/photoresist layer after isotropic etching of: (a) photoresist and Al layer and (b) SiO_2 layer

At final stage of the route isotropic etching of Al at depth of 0.22 um and SiO_2 at the depth of 0.8 um is performed for the removal of layers on a needle surface which resulting in the structure of CSG shown in Fig. 7.

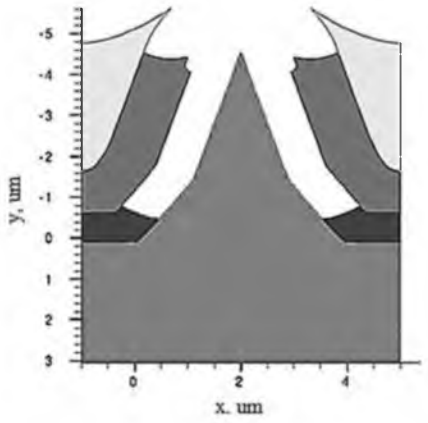

Fig. 7 Structure of CSG at the final stage of a technological route

The needle height of CSG emitter after the process simulation of all technological routes is approximately 4.63 um, and the distance between aluminium electrodes of a grid - 2.93 um. The proposed route of the formation of CSG structure allows opening of the self-combined emitter areas in a grid control layer without carrying out the expensive operations of a photolithography or chemical and mechanical polishing. On the basis of the above-stated calculations we have developed and patented the topology of the field-emission nano-cathode [3].

IV. Experiment

The PECVD SiO_2 layer with the thickness of 1.5 um was deposited on the substrate of monocrystalline silicon with orientation (100) with a diameter of 150 mm and 670 um thickness using the silane gas and nitrous oxide. After each technological operation the measurement of the structure relief was carried out by means of the optical Veeco WykoNT 9300 profilometer scanned in two directions, perpendicular to or parallel to the basic cut. The sample was subjected sequentially to temperature influences. Initially, structure of Si/SiO2 was placed in a cold chamber at a temperature - 70°C during 6 hours. Next step, heat treatment within 30 minutes at a temperature 700°C was carried out in the atmosphere of 5% of hydrogen and 95% of nitrogen (a former gas). After that, rapid thermal annealing was made at a temperature of 1150°C in a nitrogen atmosphere. The time of active stage of annealing was 15 seconds.

Relief of surface in the direction perpendicular to basic cut is shown in Fig. 8

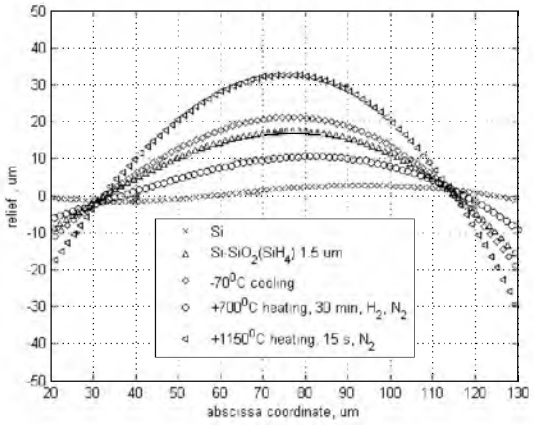

Fig. 8 Relief of surface in direction perpendicular to basic cut after carrying out temperature treatment

It can be seen from the graph that after film deposition of silicon oxide the silicon wafer became more curved. Also it is noticeable that the best processing of the sample can be carrying out by the annealing in a former gas (a minimum deflection of wafer).

Calculated curvature of the surface in the selected direction in the local area using an algorithm developed in Matlab programming environment [4]. Curvature distribution presented in Fig. 9.

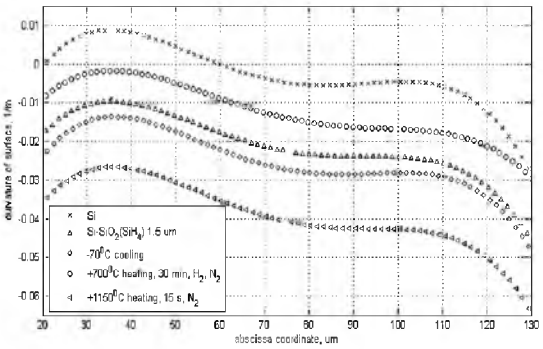

Fig. 9 The result of calculating curvature of the surface after carrying out of various temperature treatments

As follows from fig. 9 after deposition of silicon oxide films array variables curvature of the surface became completely negative. The maximum value of curvature of the surface modulus obtained after rapid annealing. Calculation of mechanical stresses carried on previously developed method [5] using the formula (1) Stoney:

$$\sigma f = \frac{E_s \cdot d_s^2}{6(1-v_S)} \cdot \frac{1}{d_f} \cdot \frac{1}{R_{after}} \quad (1),$$

where σ_f is the value of mechanical stress appearing after each technological operation, E_s is Young's modulus of the wafer material, d_s is thickness of wafer, v_s is Poisson's ratio of the wafer material, d_f is thickness of film on wafer, R_{after} is curvature radius of surface after operation.

As a result, we obtained the value of mechanical stress in local area, i.e. distribution of σ_f along the wafer in the chosen direction (Figure 10). Constant biaxial modulus ($E_s/(1-u_s)$) of the sample in the crystallographic plane (100) was $1.8 \cdot 10^{11}$ Pa [6].

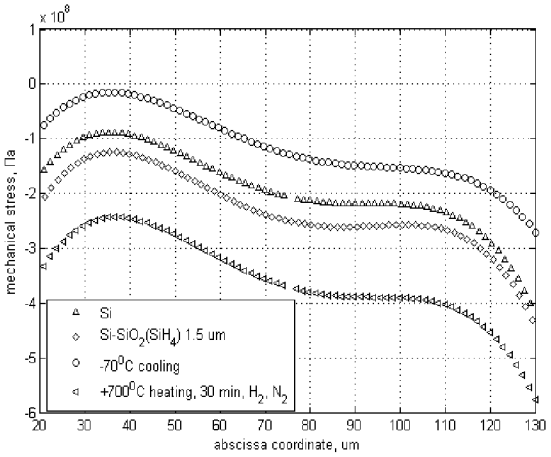

Fig. 10 The distribution of mechanical stress on wafer

Figure 10 shows that compressive stresses obtained in the film SiO_2. In this case the minimum value of the mechanical stresses modulus of approximately 100 MPa.

Analyzing the fig. 8-10 can make several conclusions. It is known that with increasing gas flow rate of silane SiH_4, decreases the mechanical stresses [7]. Besides, a penetration depth during diffusion process depends on size and mass of atoms. Atoms H_2 enough light and have a small size. Therefore, the mechanism of hydrogen atoms diffusing to the boundary Si/SiO_2 by 1.5 micron film is evident. This leads to the formation of Si-H bonds. As a result, deflection of wafer is reduced. After a high temperature annealing (1150°C) Si-H and N-H bonds are broken and hydrogen atoms leave the structure [8].

V. Conclusions

The technological route of formation of the CGS was simulated in TCAD demonstrating the possibility of low-cost technological process without photolithography or mechanochemical polishing. It was found that the best temperature regime of is carrying out the sample treatment annealing gas former, since level of mechanical stresses in the silicon oxide film and deflection of sample is minimal.

Acknowledgment

This work was supported by Ministry of Education and Science of Russian Federation (within the agreement № 14.578.21.0188, id RFMEF57816X0188).

References

[1] Kevin Cheng, Yi-Ping Chou, Meng-Jey Youh, Yih-Ming Liu, MingDer Ger , Kung-Hsu Hou and Nen-Wen Pu , "Fabrication and Simulation of Self-Focusing Field X-ray tubes," *Applied Sciences,* vol. 5, pp.942-954, 2015

[2] (2015) Sentaurus TCAD. Available: http://www.synopsys.com/tools/tcad/Pages/default.aspx

[3] E.E. Gusev, N.A. Djuzhev, M.A. Makhiboroda and V.I. Zolotarev, "The topology of field-emission nano-cathode," RF, Patent, №2016630035, 2016.

[4] E.E. Gusev, A.A. Dedkova, N.A. Djuzhev and M.U. Chinenkov, "The program of analysis of a relief for purpose of calculation of curvature of a surface in the chosen direction on a silicon wafer," RF, Patent, №2016611518, 2016

[5] N.A. Djuzhev, A.A. Dedkova, E.E. Gusev and A.V.Novak, "Method measurement mechanical stresses in thin films on wafer using an optical profilometer," *Proceedings of universities. Electronics.* vol. 4, pp. 367 – 372, 2016

[6] A. K.Sinha, H. J. Levinstein and T. E. Smith, "Thermal stresses and cracking resistance of dielectric films (SiN, Si_3N_4, and SiO_2) on Si substrates," *Journal of Applied Physics*. vol. 49, pp. 2423-2426, 1978.

[7] Carlos Dotinguez, J. A. Rodriguez, F. J. Munoz and N. Zine, "The effect of rapid thermal annealing on properties of plasma enhanced CVD silicon oxide films," *Thin Solid Films*, pp.202-206, 1999

[8] Feridun, "Silicon oxynitride layers for applications in optical waveguides," M. thesis, Institute of Engineering and Science of Bilkent University, Turkey, September 2000